

ENTRY	NUMBER	ROUTING DESTINATION
A	908 979 XXXX	STATION NUMBER
B	908 852 XXXX	CENTRAL OFFICE 852
C	908 XXX XXXX	908 TANDEM SWITCH
D	XXX XXX XXXX	LONG DISTANCE POINT-OF-PRESENCE

FIG. 1
PRIOR ART

ENTRY	NUMBER	NUMBER	ROUTING DESTINATION
A	908 XXX XXXX		EXAMINE LIST THAT FOLLOWS
A.a		908 979 XXXX	STATION NUMBER
A.b		908 852 XXXX	CENTRAL OFFICE 852
A.c		908 XXX XXXX	908 TANDEM SWITCH
B	XXX XXX XXXX		LONG DISTANCE POINT-OF-PRESENCE

FIG. 2

ENTRY	NUMBER	LEVEL	ROUTING DESTINATION
A	908 979 XXXX	3	STATION NUMBER
B	908 852 XXXX	3	CENTRAL OFFICE 852
C	908 XXX XXXX	2	908 TANDEM SWITCH
D	XXX XXX XXXX	1	LONG DISTANCE POINT-OF-PRESENCE

FIG. 3

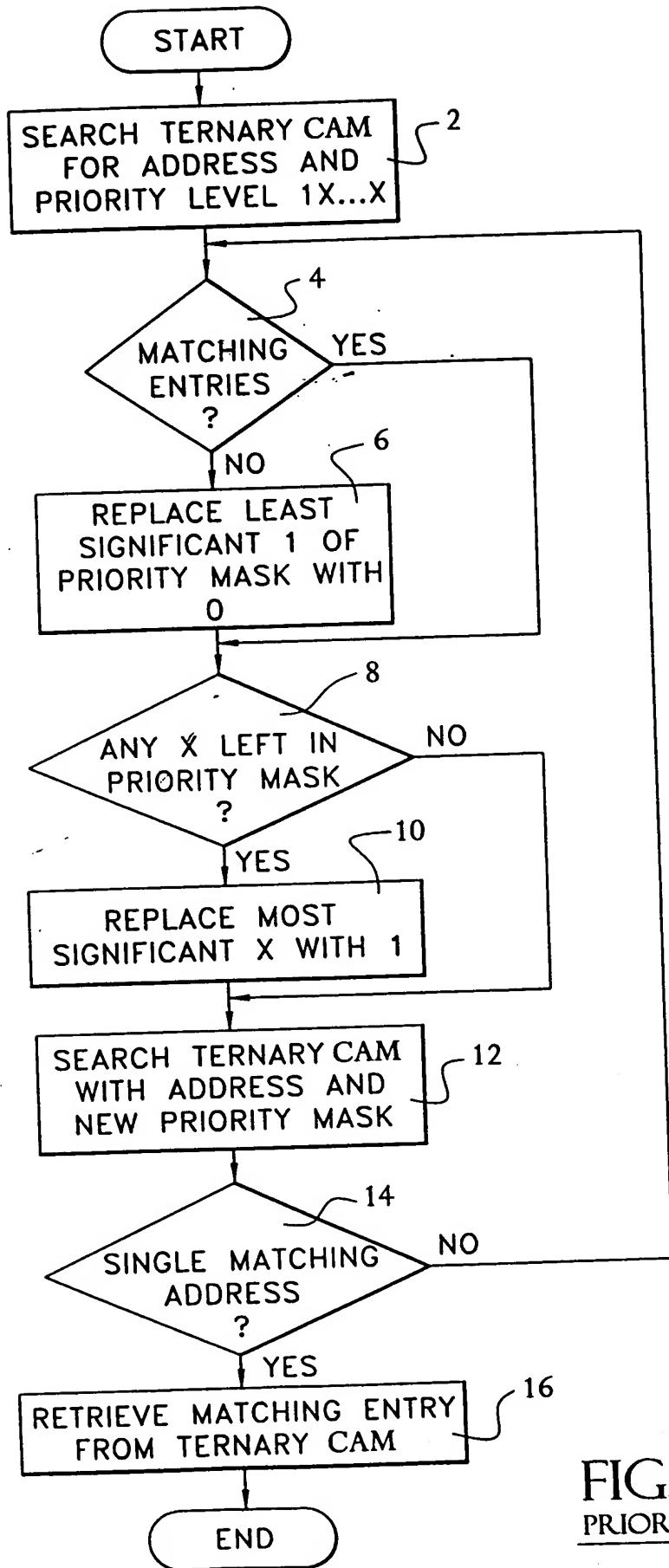


FIG. 4
PRIOR ART

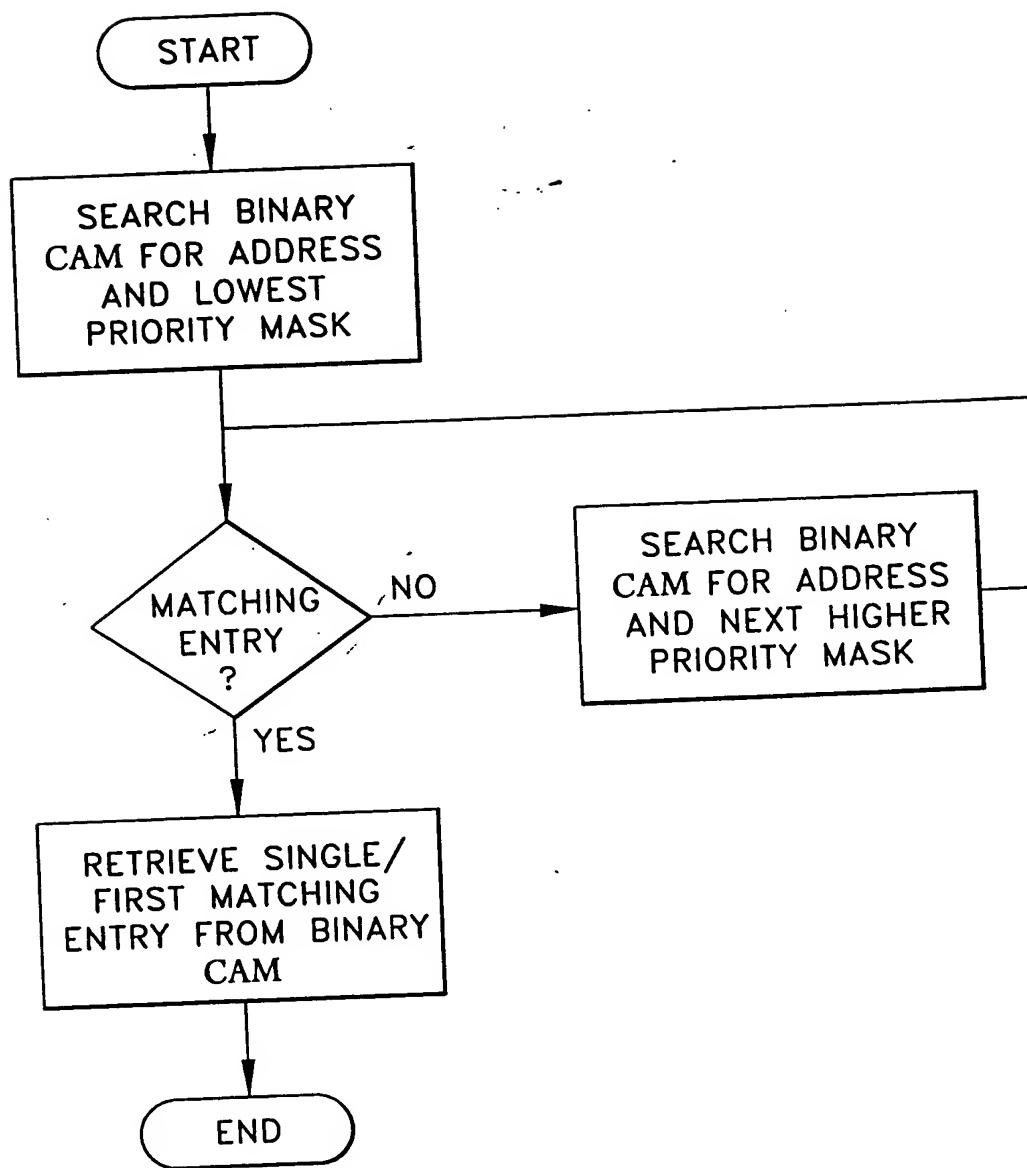


FIG. 5
PRIOR ART

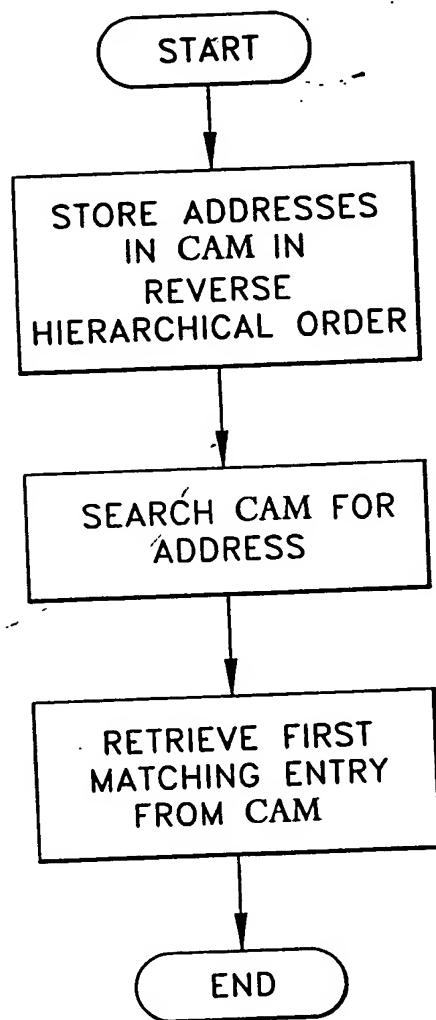


FIG. 6
PRIOR ART

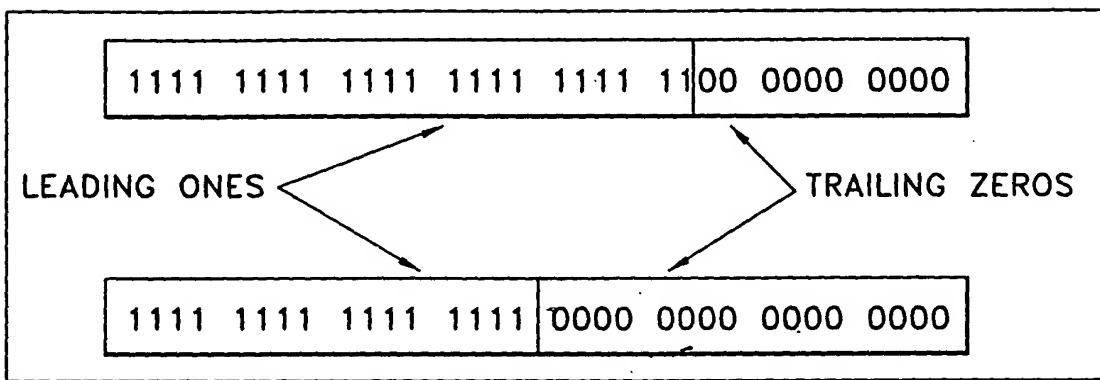


FIG. 7

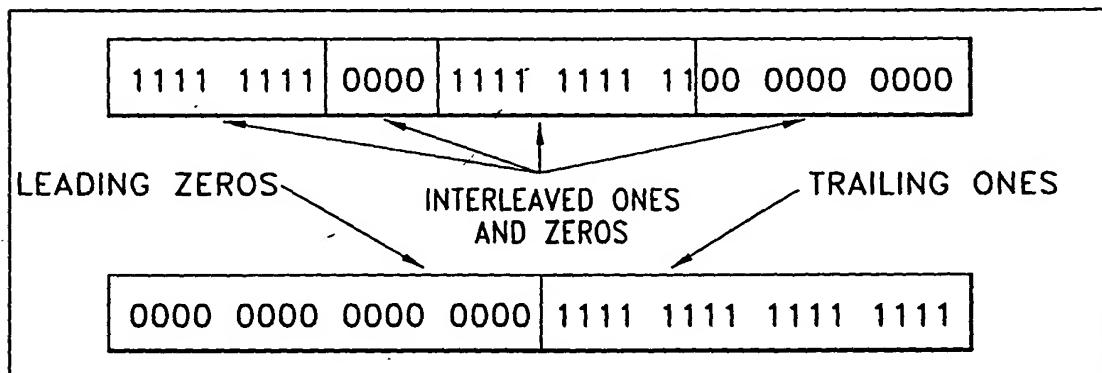


FIG. 8

ADDRESS	MASK
C0.18.OC.15	FF.FF.FF.FF/32
C0.18.OC.10	FF.FF.FF.F0/28
C0.18.OC.00	FF.FF.FC.00/22
C0.18.00.00	FF.FF.00.00/16

FIG. 9

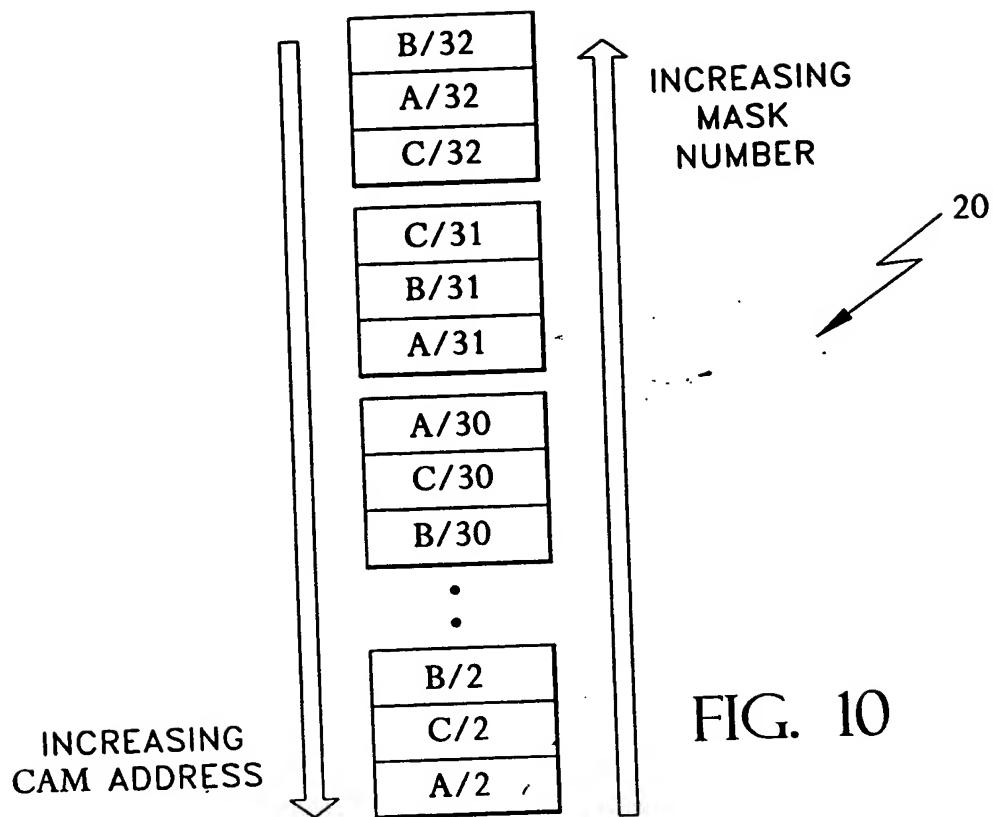


FIG. 10

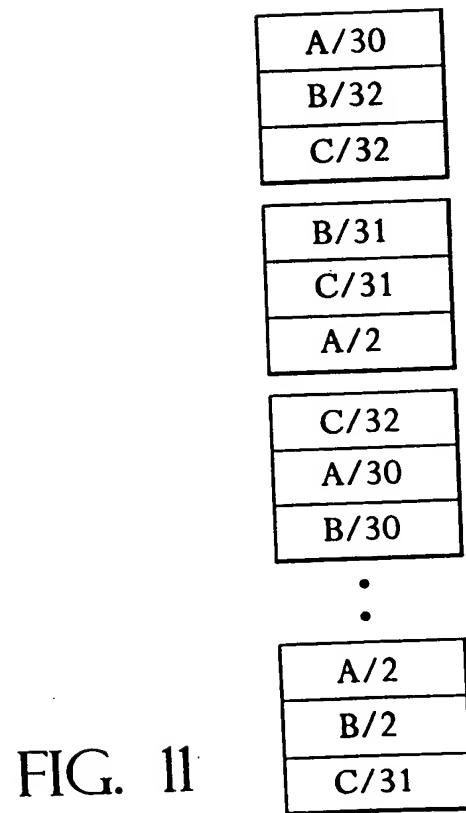


FIG. 11

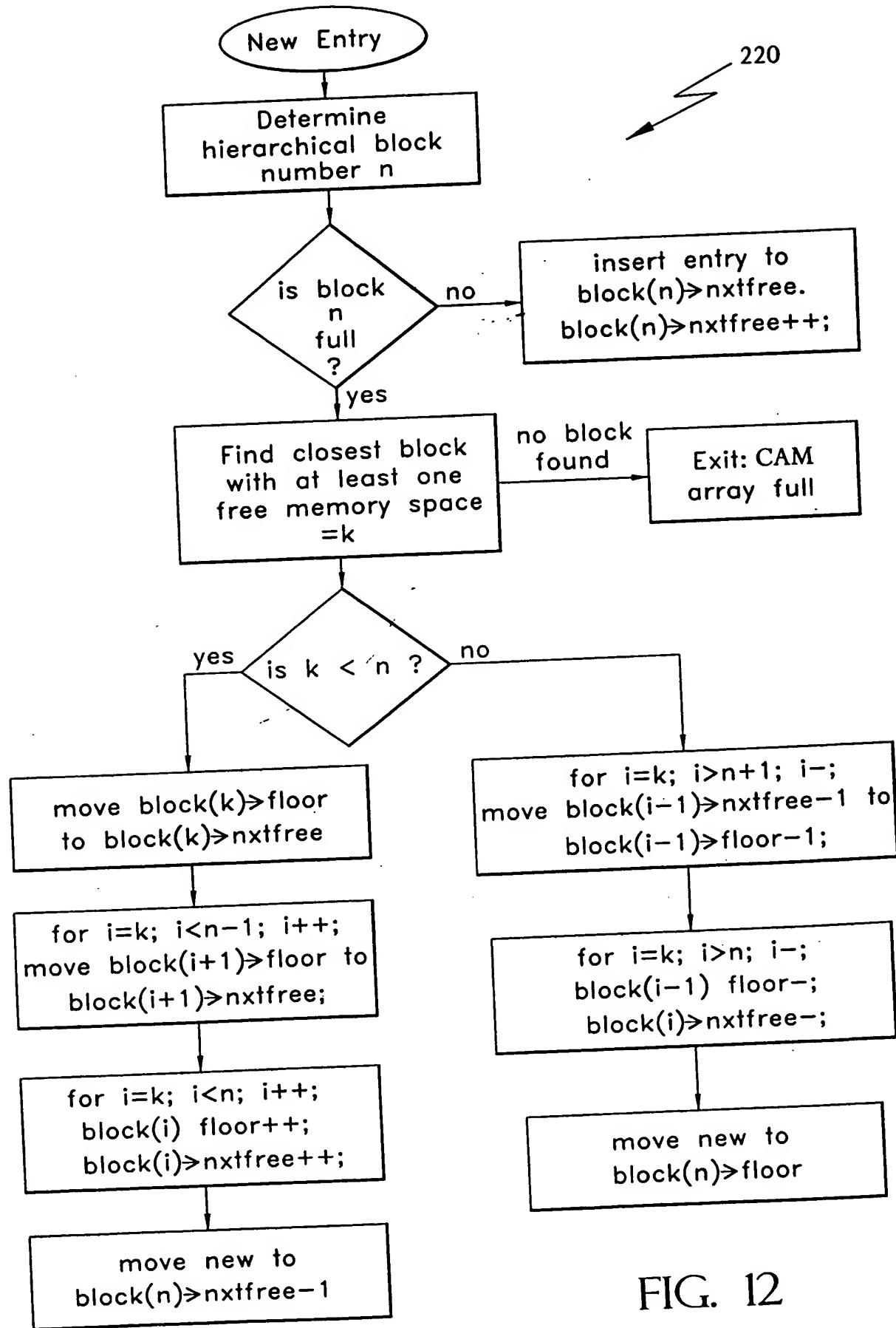


FIG. 12

FIG. 13

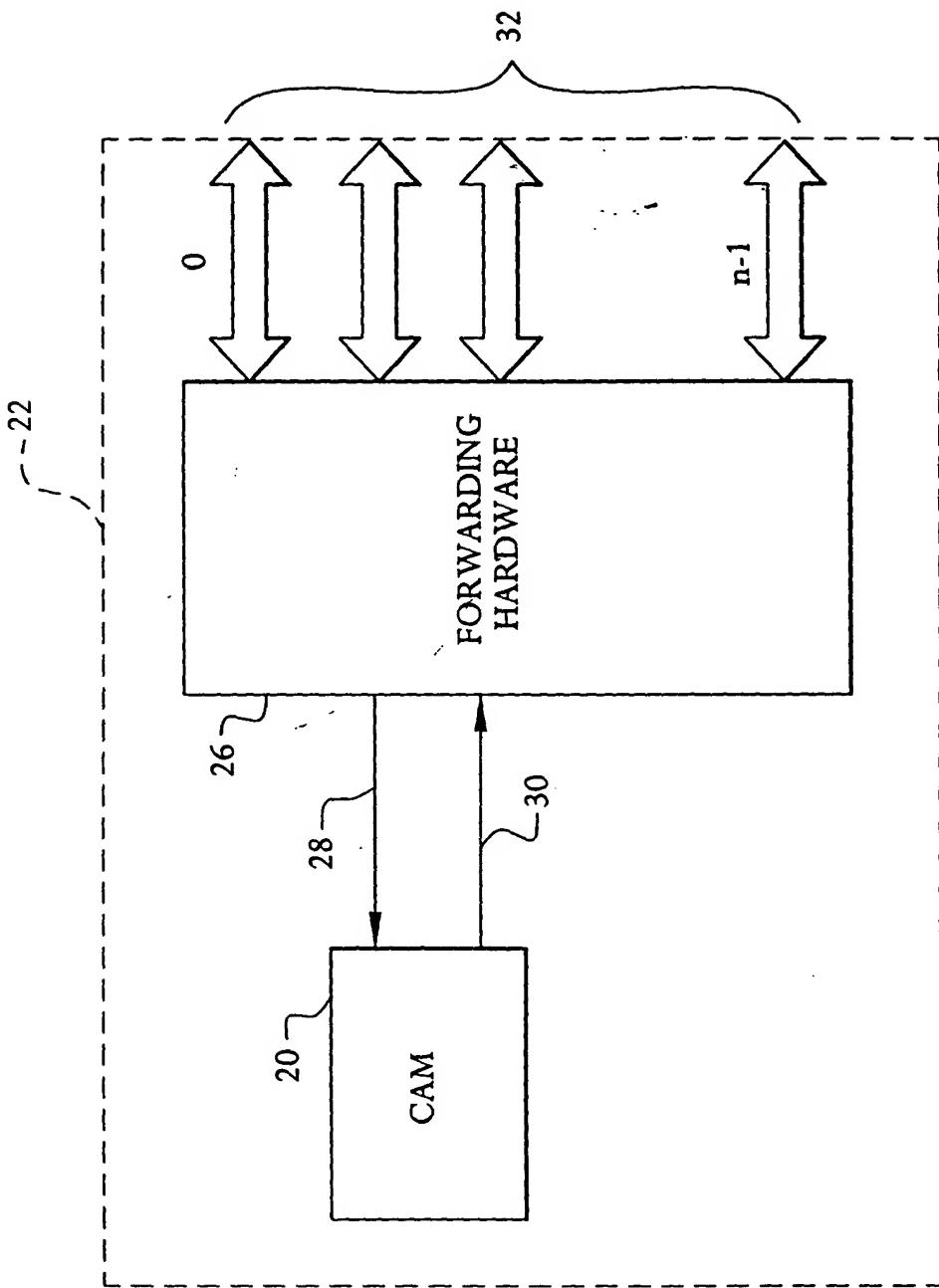
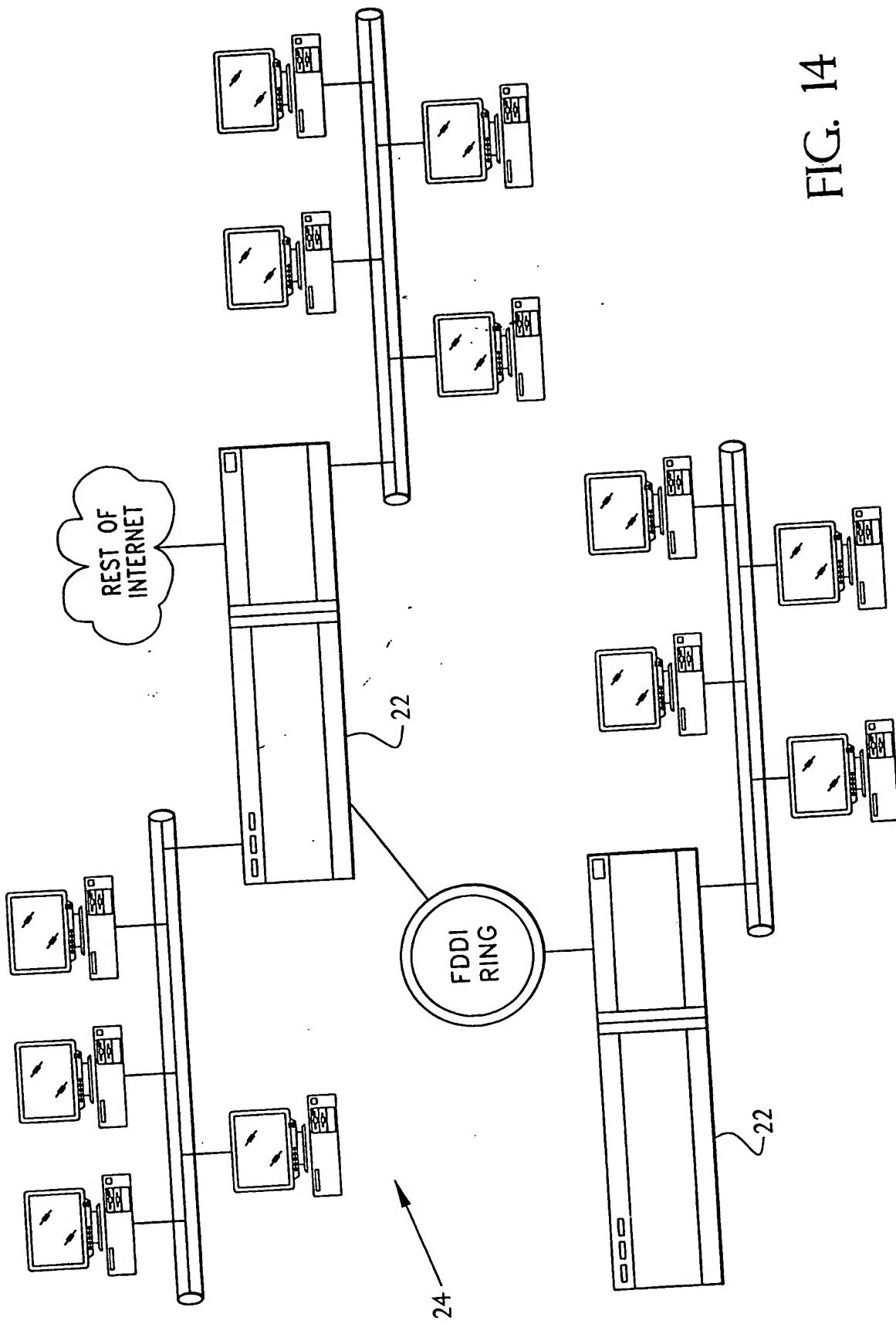
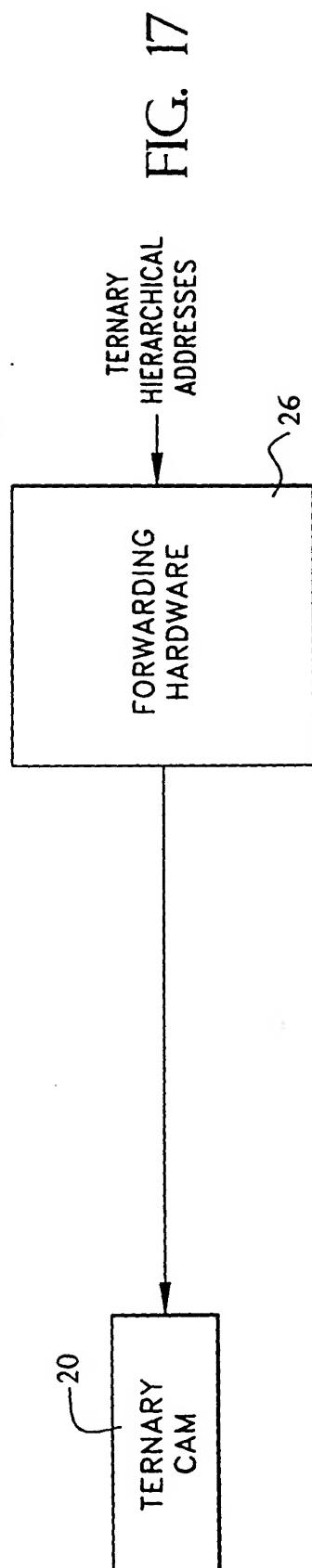
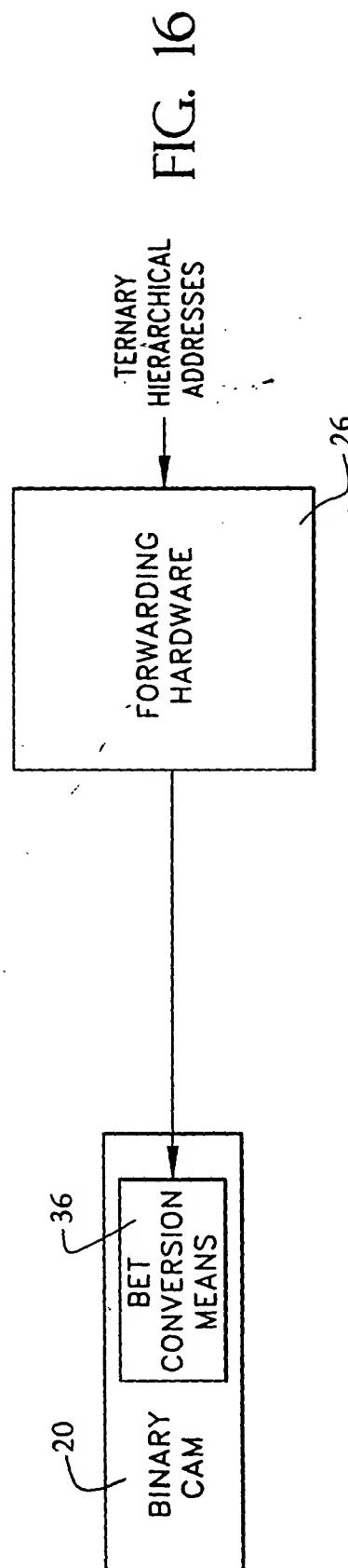
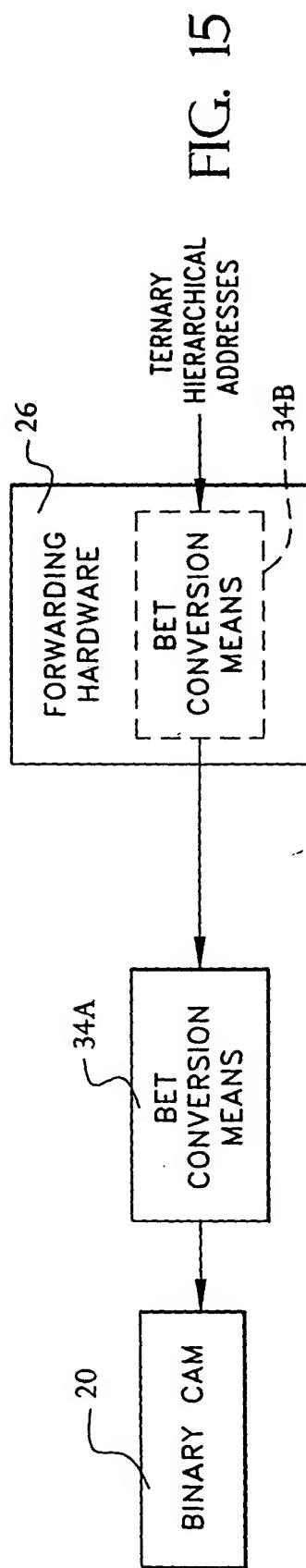


FIG. 14





63	32	31	0
ADDR AND MASK		(IADDR) AND MASK	
CO.18.OC.15			3F.E7.F3.EA

FIG. 18

TERNARY	BINARY ENCODED
0	01
1	10
X	00

FIG. 19

38	COMPARAND BITS	10(1)	10(1)	10(1)
40	MASK BITS	10	10	10
	CAM BITS	00(X)	01(0)	10(1)
	RESULT	MATCH	NO-MATCH	MATCH

FIG. 20

COMPARAND BIT	0	1	0	1	0	1	0	1
MASK BIT	0	0	1	1	0	0	1	1
CAM BIT	0	0	0	0	1	1	1	1
RESULT	MATCH	NO-MATCH	MATCH	MATCH	NO-MATCH	MATCH	MATCH	MATCH

FIG. 21

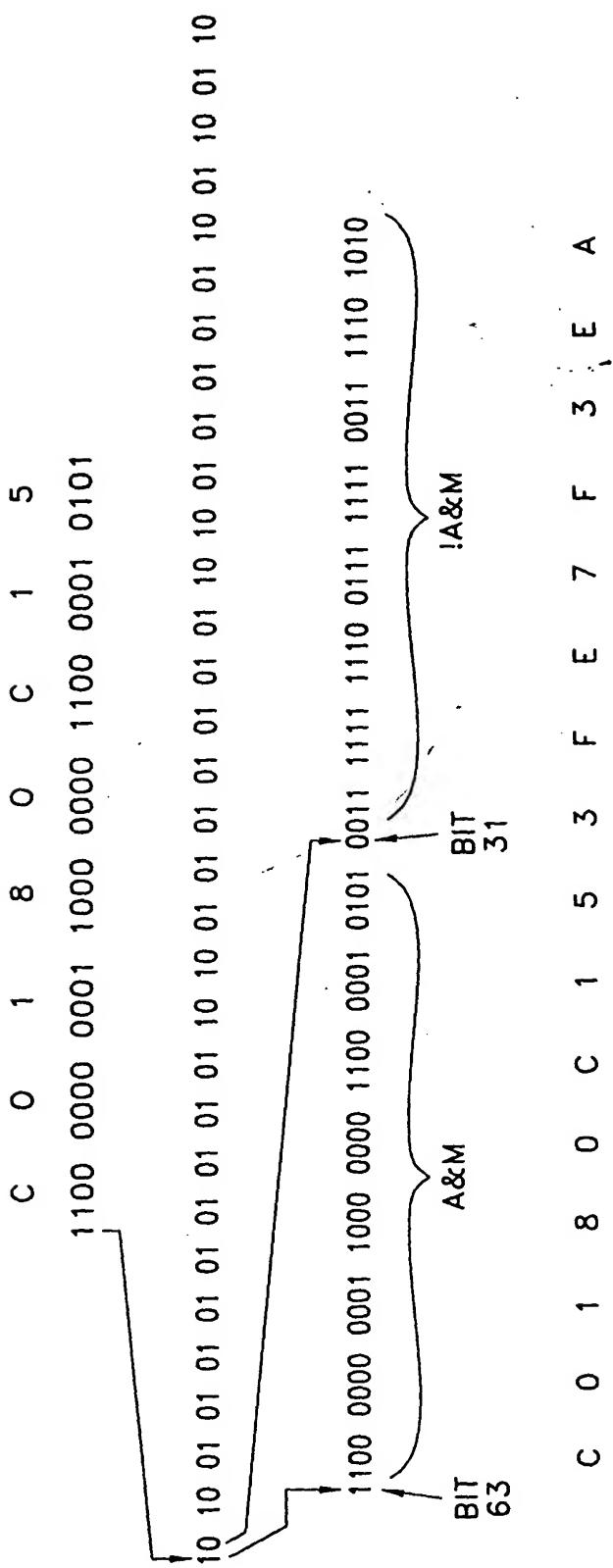


FIG. 22

1100 0000 0001 1000 0000 1100 0001 0101	C0180C15
0011 1111 1110 0111 1111 0011 1110 1010	3FE7F3EA

FIG. 23

ENTRY	IP ADDRESS	IP MASK	CAM BITS [63:32]	CAM BITS [31:0]
1	CO.18.OC.15	FF.FF.FF.FF	CO.18.OC.15	3F.E7.F3.EA
2	CO.18.OC.10	FF.FF.FF.F0	CO.18.OC.10	3F.E7.F3.E0
3	CO.18.OC.00	FF.FF.FC.00	CO.18.OC.00	3F.E7.F0.00
4	CO.18.00.00	FF.FF.F0.00	CO.18.00.00	3F.E7.00.00

FIG. 24

COMPARAND REGISTER	1100 0000 0001 1000 0000 1100 0001 0101 0011 1111 1110 0111 1111 0011 1110 1001
MASK REGISTER	1100 0000 0001 1000 0000 1100 0001 0101 0011 1111 1110 0111 1111 0011 1110 1001
CAM ENTRY	1100 0000 0001 1000 0000 1100 0000 0000 0011 1111 1110 0111 1111 0000 0000 0000
RESULT	xxxx yyyy yyyy xxxx yyyy yyyy xxxx xxxx yyyy yyyy xxxx yyyy xxxx

FIG. 25

NOTES:
1. x = THE RESULT WAS A "DON'T CARE" MATCH.
2. y = THE RESULT WAS A NORMAL BINARY MATCH.

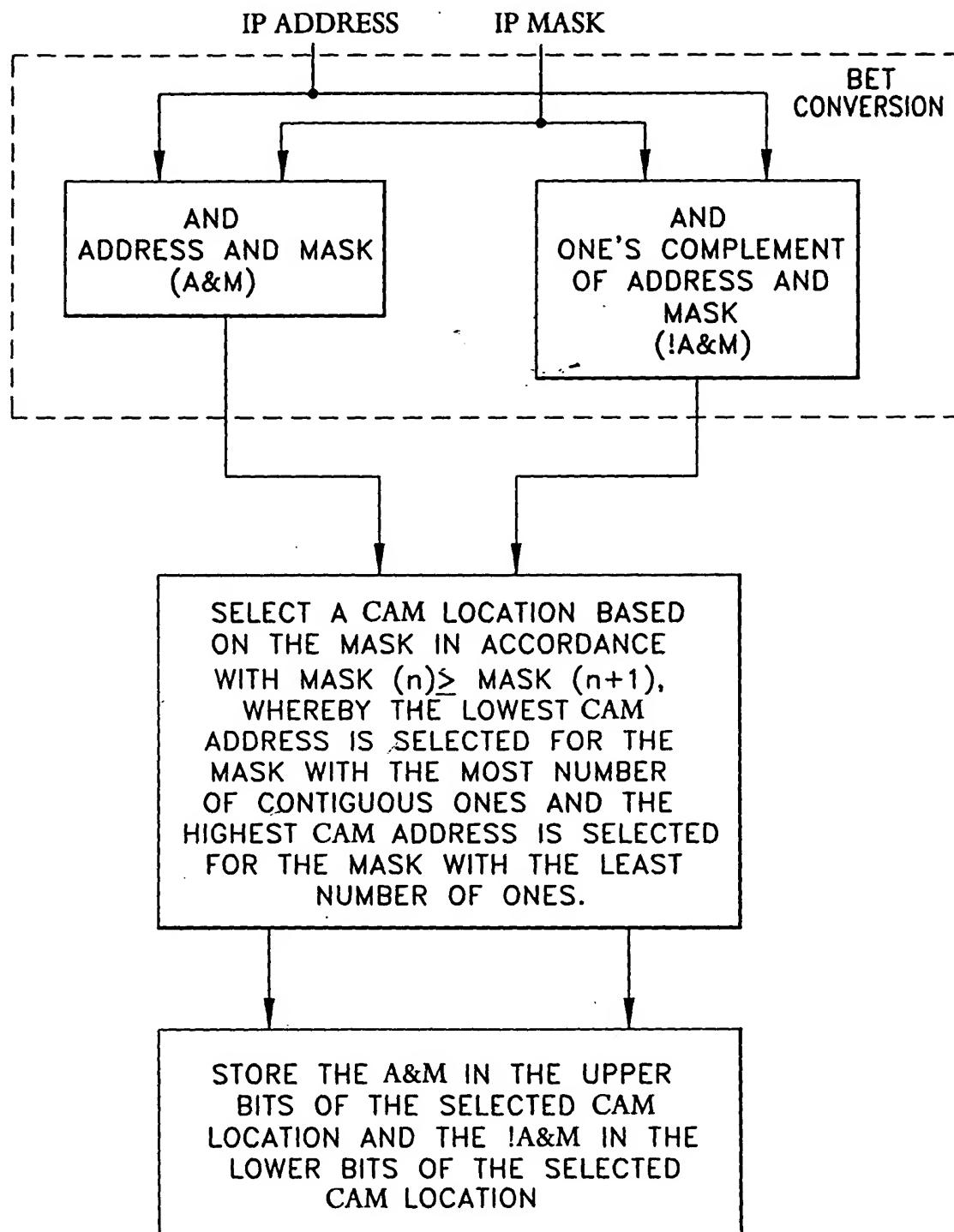


FIG. 26

LOAD THE UPPER BITS OF THE COMPARAND REGISTER WITH ADDRESS AND LOAD THE LOWER BITS OF THE COMPARAND REGISTER WITH !ADDRESS

LOAD THE UPPER BITS OF THE CAM MASK REGISTER WITH ADDRESS AND LOAD THE LOWER BITS OF THE CAM MASK REGISTER WITH !ADDRESS

IS THE CAM MASK REGISTER BIT A "1" ?

YES

"DON'T CARE EXISTS;
CONSIDER COMPARAND REGISTER BIT AND CORRESPONDING CAM ENTRY BIT FORM A "MATCH";

NO

COMPARE THE COMPARAND REGISTER BIT WITH ITS CORRESPONDING CAM ENTRY BIT: ARE THEY IDENTICAL ?

YES

MATCH;

NO

NO MATCH

GO TO NEXT BIT IN CAM MASK REGISTER

YES

ARE THERE ANY CAM MASK REGISTER BITS ?

NO

END

FIG. 27

f=FLOOR ENTRY
n=NEXT-FREE

ENTRY
/#=MASK OR
BLOCK NUMBER
NEW ENTRY

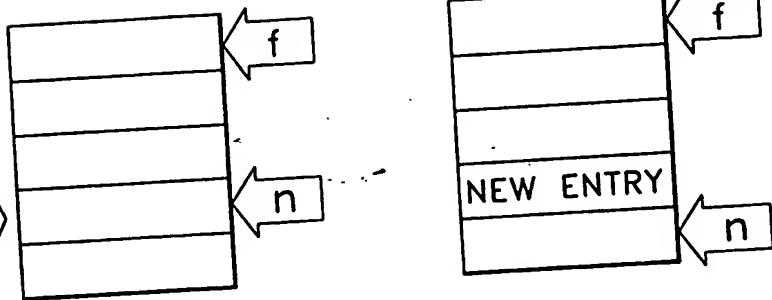


FIG. 28

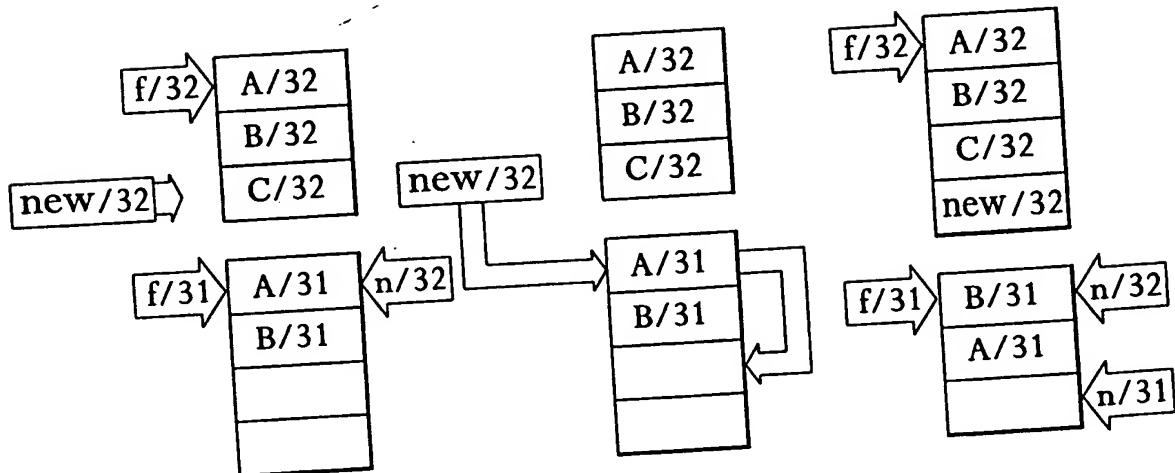


FIG. 29a

FIG. 29b

FIG. 29c

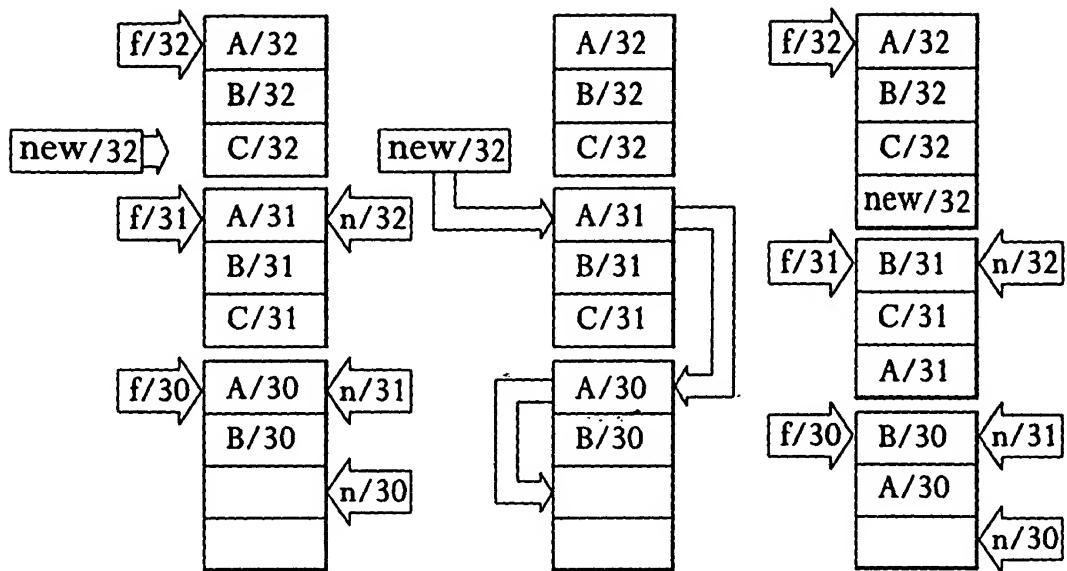


FIG. 30a

FIG. 30b

FIG. 30c

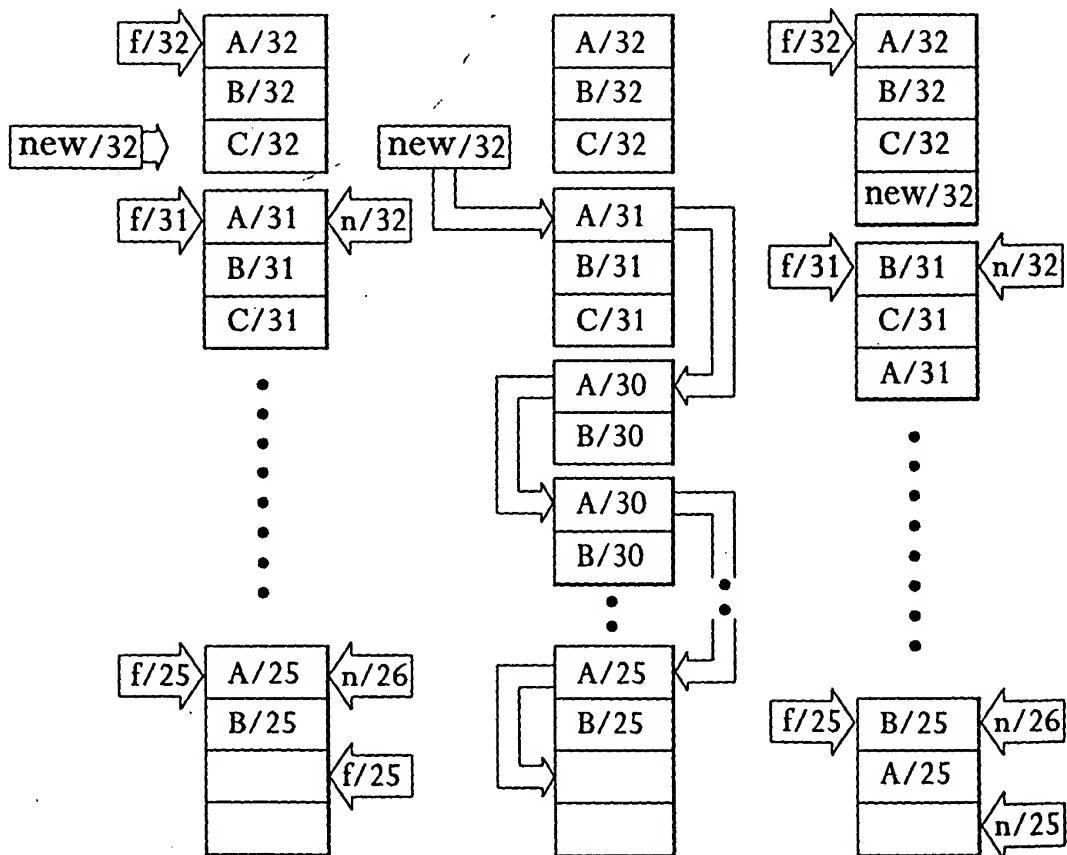


FIG. 31a

FIG. 31b

FIG. 31c

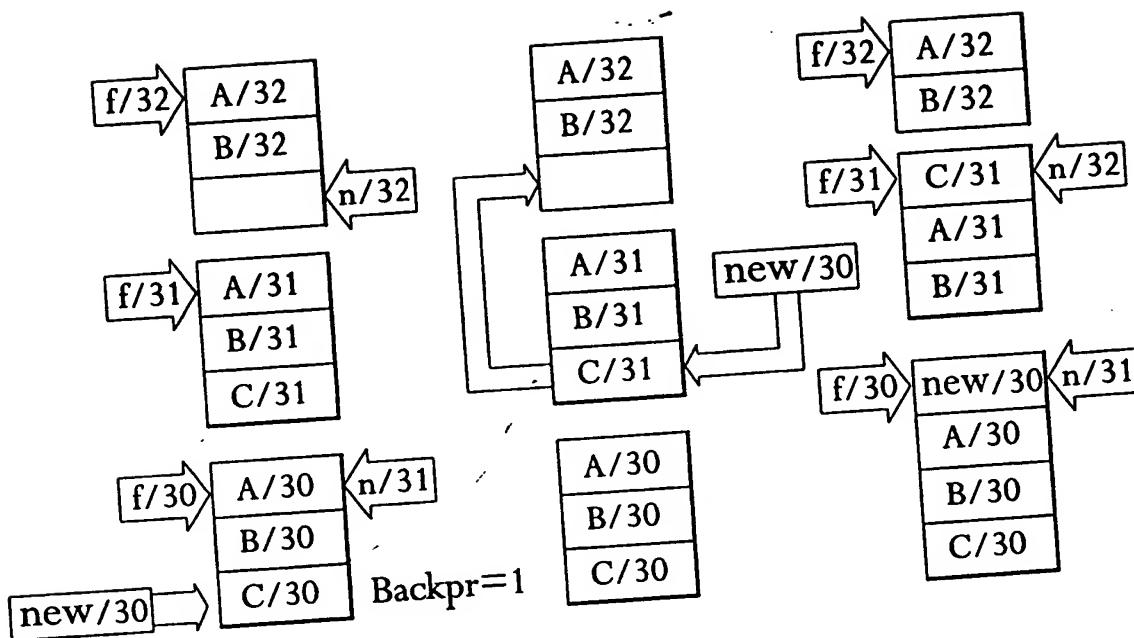
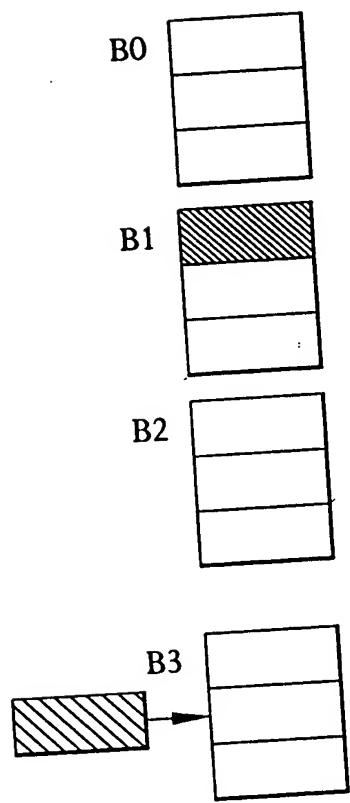


FIG. 32a

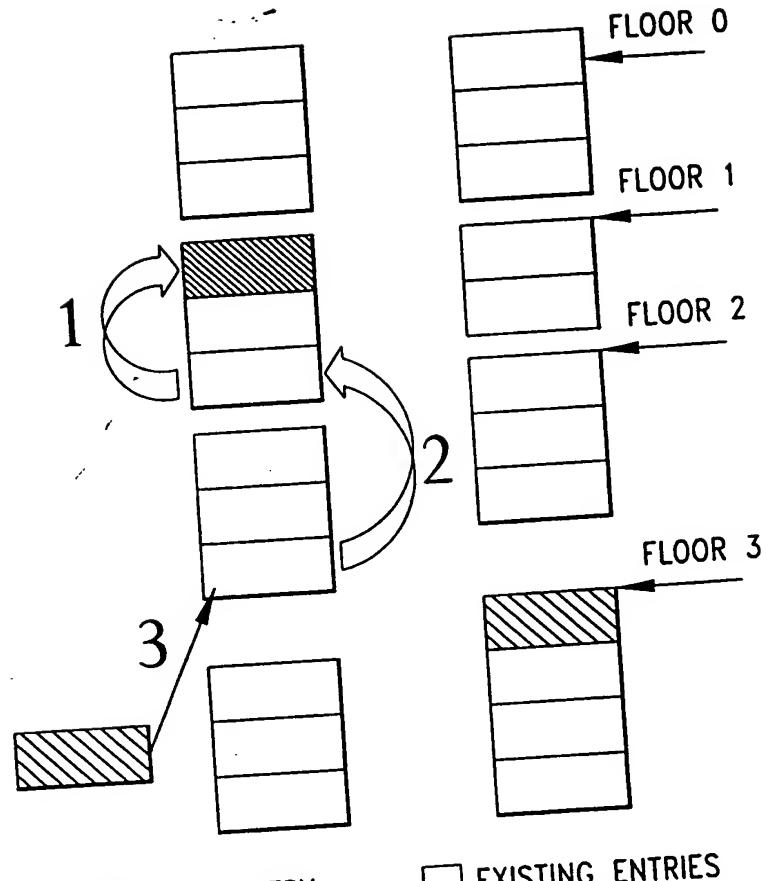
FIG. 32b

FIG. 32c



■ NEW ENTRY

FIG. 33a



■ FREE ENTRY

FIG. 33b

□ EXISTING ENTRIES

FIG. 33c

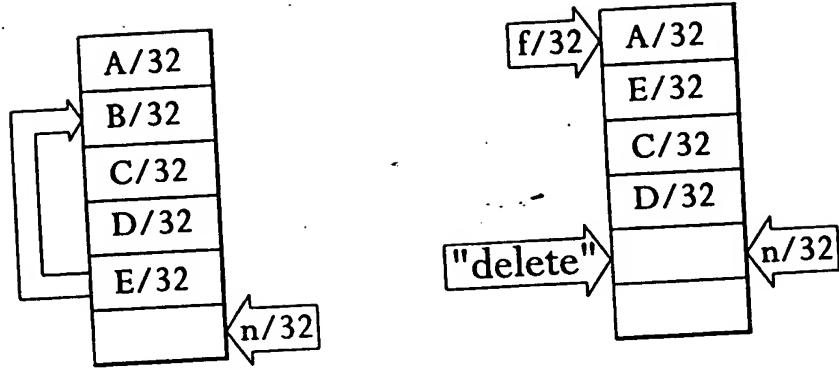


FIG. 34a

FIG. 34b

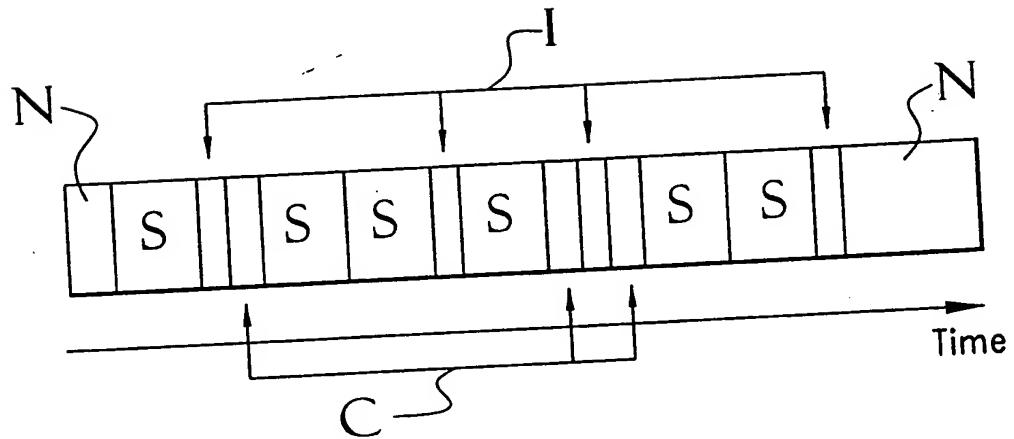


FIG. 35